What is Claimed is:

1. A circuit for converting an analog input at an input terminal to a digital output at an output terminal, the circuit comprising:

an analog chopper circuit having an input coupled to the input terminal, and providing an output at a first predetermined rate f_{chop};

a first terminal and a second terminal, wherein a customized buffer/amplifier may be placed across the first and second terminals such that the output of the analog chopper at a first predetermined rate f_{chop} is received at the first terminal and the output of the customized buffer/amplifier is received at the second terminal;

a quantizer circuit having an input coupled to the second terminal, and providing an output at a second predetermined rate f_{quant};

a first digital filter and first decimator having an input coupled to the output of the quantizer circuit, and providing an output at a rate f_{quant} divided by M (f_{quant}/M);

a second digital filter having an input coupled to the output of the first digital filter and first decimator; and

a second decimator having an input coupled to the output of the second digital filter, and providing the digital output at a rate f_{quant} divided by M×P ($f_{quant}/(M\times P)$).

2. The circuit of claim 1, wherein the quantizer is a Δ-Σ modulator.

3. The circuit of claim 1, wherein the quantizer is a single-bit Δ-Σ modulator.

4. The circuit of claim 1, wherein the quantizer is a multi-bit Δ-Σ modulator.

5. The circuit of claim 1, wherein the quantizer is a successive approximation quantizer.

6. The circuit of claim 1, wherein the quantizer is a flash quantizer.

7. The circuit of claim 1, wherein the quantizer is a pipelined quantizer.

8. The circuit of claim 1, wherein the first predetermined frequency f_{chop} equals the second predetermined frequency f_{quant} divided by two times M ($f_{chop} = f_{quant}/(2\times M)$).

9. The circuit of claim 1, wherein P = 2.

10. A circuit for converting a differential analog input at a pair of differential input terminals to a digital output at an output terminal, the circuit comprising:

a cross-coupled switch having a first input coupled to one of the pair of differential input terminals and a second input coupled to the other of the pair of differential input terminals, and providing a differential output at a first predetermined rate f_{chop};

a first terminal and a second terminal, wherein a customized buffer/amplifier may be placed across the first and second terminals such that the output of the cross-coupled switch at a first

predetermined rate f_{chop} is received at the first terminal and the output of the customized buffer/amplifier is received at the second terminal;

a quantizer circuit having a differential input coupled to the second terminal, and providing an output at a second predetermined rate f_{quant};

a first digital filter and first decimator having an input coupled to the output of the quantizer circuit, and providing an output at a rate f_{quant} divided by M (f_{quant} /M);

a second digital filter having an input coupled to the output of the first digital filter and first decimator; and

a second decimator having an input coupled to the output of the second digital filter, and providing the digital output at a rate f_{quant} divided by M times P (f_{quant}/(M*P).

11. The circuit of claim 10, wherein the quantizer is a Δ-Σ modulator.

12. The circuit of claim 10, wherein the quantizer is a single-bit Δ-Σ modulator.

13. The circuit of claim 10, wherein the quantizer is a multi-bit Δ-Σ modulator.

14. The circuit of claim 10, wherein the quantizer is a successive approximation quantizer.

15. The circuit of claim 10, wherein the quantizer is a flash quantizer.

16. The circuit of claim 10, wherein the quantizer is a pipelined quantizer.

17. The circuit of claim 10, wherein the first predetermined frequency f_{chop} equals the second predetermined frequency f_{quant} divided by two times M ($f_{chop} = f_{quant}/(2*M)$).

18. The circuit of claim 10, wherein P = 2.

19. A circuit for converting a differential analog input at an input terminal to a digital output at an output terminal, the circuit comprising:

an analog multiplier having a first input coupled to the input terminal, and providing an output at a first predetermined rate f_{chop};

a first terminal and a second terminal, wherein a customized buffer/amplifier may be placed across the first and second terminals such that the output of the analog multiplier at a first predetermined rate f_{chop} is received at the first terminal and the output of the customized buffer/amplifier is received at the second terminal;

a quantizer circuit having an input coupled to the second terminal, and providing an output at a second predetermined rate f_{quant};

a first digital filter and first decimator having an input coupled to the output of the quantizer circuit, and providing an output at a rate f_{quant} divided by M (f_{quant}/M);

a second digital filter having an input coupled to the output of the first digital filter and first decimator; and

a second decimator having an input coupled to the output of the second digital filter, and providing the digital output at a rate f_{quant} divided by M times P ($f_{quant}/(M*P)$.

20. The circuit of claim 19, wherein the quantizer is a Δ-Σ modulator.

21. The circuit of claim 19, wherein the quantizer is a single-bit Δ-Σ modulator.

22. The circuit-of claim 19, wherein the quantizer is a multi-bit Δ-Σ modulator.

23. The circuit of claim 19, wherein the quantizer is a successive approximation quantizer.

24. The circuit of claim 19, wherein the quantizer is a flash quantizer.

25. The circuit of claim 19, wherein the quantizer is a pipelined quantizer.

26. The circuit of claim 19, wherein the first predetermined frequency f_{chop} equals the second predetermined frequency f_{quant} divided by two times M ($f_{chop} = f_{quant}/(2*M)$).

27. The circuit of claim 19, wherein P = 2.

28. A circuit for converting a differential analog input at a pair of differential input terminals to a digital output at an output terminal, the circuit comprising:

a multiplexer having a first input coupled to one of the pair of differential input

terminals and a second input coupled to the other of the pair of differential input terminals, and providing a differential output at a first predetermined rate f_{chop};

a first terminal and a second terminal, wherein a customized buffer/amplifier may be placed across the first and second terminals such that the output of the multiplexer at a first predetermined rate f_{chop} is received at the first terminal and the output of the customized buffer/amplifier is received at the second terminal;

a quantizer circuit having a differential input coupled to the second terminal, and providing an output at a second predetermined rate f_{quant};

a first digital filter and first decimator having an input coupled to the output of the quantizer circuit, and providing an output at a rate f_{quant} divided by M (f_{quant}/M);

a second digital filter having an input coupled to the output of the first digital filter and first decimator; and

a second decimator having an input coupled to the output of the second digital filter, and providing the digital output at a rate f_{quant} divided by M times P ($f_{quant}/(M*P)$.

29. A method of converting an analog input at an input terminal to a digital output at an output terminal, the method comprising:

chopping the analog input with a chop signal to provide a chopped signal at a first predetermined rate f_{chop};

receiving the chopped signal at a first predetermined rate f_{chop} at a first terminal;

providing for a customized buffer/ amplifier to be placed across the first terminal and a second terminal such that the chopped signal at a first predetermined rate f_{chop} is received at the input of the customized buffer/amplifier and the output of the customized buffer/amplifier is received at the second terminal;

receiving the output of the customized buffer/amplifier at the second terminal;

quantizing the chopped signal the received output of the customized buffer/amplifier to provide a quantized signal at a second predetermined rate f_{quant};

digitally filtering the quantized signal to provide a first filtered signal;

decimating the first filtered signal by a factor M to provide a first decimated signal at a rate f_{quant} divided by M (f_{quant}/M);

digitally filtering the first decimated filter to provide a second filtered signal; and

decimating the second filtered signal by a factor P to provide the digital output at a rate f_{quant} divided by M times P ($f_{quant}/(M*P)$).

30. The method of claim 29, wherein the quantizing step comprises quantizing the chopped signal by Δ-Σ modulation.

31. The method of claim 29, wherein the quantizing step comprises quantizing the chopped signal by single-bit Δ-Σ modulation.

32. The method of claim 29, wherein the quantizing step comprises quantizing the chopped signal by multi-bit Δ-Σ modulation.

33. The method of claim 29, wherein the quantizing step comprises quantizing the chopped signal by successive approximation quantization.

34. The method of claim 29, wherein the quantizing step comprises quantizing the chopped signal by flash quantization.

35. The method of claim 29, wherein the quantizing step comprises quantizing the chopped signal by pipelined quantization.

36. The method of claim 29, wherein the first predetermined frequency f_{chop} equals the second predetermined frequency f_{quant} divided by two times M ($f_{chop} = f_{quant} / (2*M)$).

37. The method of claim 29, wherein $P = 2$.